semiconductor device

CROSS-REFERENCE TO RELATED APPLICATION

This application is based upon and claims the benefit of priority from Japanese Patent Application No. 2015-206533; filed October 20, 2015; the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a semiconductor device.

BACKGROUND

A semiconductor device provided with a non-volatile memory and a controller is provided.

An example of related art includes JP-A-2009-86830.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view illustrating a system with a built-in semiconductor device according to a first embodiment.

FIG. 2 is a partially cutaway perspective view illustrating a state where the semiconductor device is mounted on a host device.

FIG. 3 is a partially cutaway cross-sectional view of a tablet portion constituting the host device.

FIGS. 4A to 4C illustrate views of the semiconductor device according to the first embodiment, FIG. 4A is a front view, FIG. 4B is a rear view, and FIG. 4C is a side view.

FIG. 5 is a block diagram illustrating a system configuration of the semiconductor device according to the first embodiment.

FIG. 6 is a cross-sectional view illustrating a NAND memory and a controller.

FIG. 7 is a block diagram illustrating a system configuration of the controller.

FIG. 8 is a diagram illustrating an example of a connection relationship between the semiconductor devices according to the first embodiment.

FIG. 9 is a flowchart illustrating an example of the operation of the controller during data saving of the semiconductor device according to the first embodiment.

FIG. 10 is a diagram illustrating another example of a connection relationship between the semiconductor devices according to the first embodiment.

FIGS. 11A to 111C illustrate views of a semiconductor device according to a second embodiment, FIG. 11A is a front view, FIG. 11B is a rear view, and FIG. 11C is a side view.

FIG. 12 is a diagram illustrating a connection example between the semiconductor devices according to the second embodiment.

DETAILED DESCRIPTION

[0004]Embodiments enables efficient data saving of a semiconductor device.

[0005]In general, according to one embodiment, a semiconductor device is provided which includes a first substrate on which an interface unit connectable to a host device is provided; a first memory that is mounted on the first substrate; a first controller that is mounted on the first substrate and includes a control unit which controls the first memory, and a switching unit which switches an operation mode in response to a command from the host device; and a first connecting portion that is provided on the first substrate, and is electrically connected to the first memory and the first controller, in which the first controller that accesses an external second memory through the first connecting portion, and reads data stored in the second memory, in response to the switching by the switching unit.

[0007]Hereinafter, embodiments will be described with reference to the drawings.

[0008]In the present specification, some elements are denoted by a plurality of exemplary expressions. In addition, these exemplary expressions are merely examples, and the elements may be expressed in other expressions. The elements which are denoted by a plurality of expressions may be expressed in other expressions.

[0009]Further, the drawings are schematic, and the relationship between the thickness and the planar dimension, and the ratio between the thicknesses of respective layers may differ from actual relationship and ratio. With respect to some components, the dimensional relationships and the ratios are different from each other among the drawings. Furthermore, for convenience of explanation, some components and configurations may be omitted in the drawings.

First embodiment

[0010]FIGS. 1 to 3 illustrate a semiconductor device 1 according to a first embodiment and a system 100 with the built-in semiconductor device 1. The system 100 is an example of “electronic equipment”. The semiconductor device 1 is an example of “a semiconductor module” and “a semiconductor memory device”. The semiconductor device 1 according to the present embodiment is, for example, a memory system such as a solid state drive (SSD), but is not limited thereto.

[0011]As illustrated in FIG. 1, the semiconductor device 1 is built as a storage device into the system 100 such as a server. The system 100 includes the semiconductor device 1, and a host device 2 including the semiconductor device 1 mounted therein. The host device 2 includes, for example, a plurality of connectors 3 (for example, slots) which are opened upward.

[0012] A plurality of semiconductor devices 1 are respectively mounted in the connectors 3 of the host device 2, and the semiconductor devices 1 are arranged and supported with each other in a standing state in a substantially vertical direction. According to such a configuration, the plurality of semiconductor devices 1 can compactly be arranged and mounted, thereby allowing a reduction in the size of the host device 2.

[0013]For example, the semiconductor device 1 may be used as a storage device of electronic equipment such as a notebook portable computer, a tablet terminal, and the other detachable notebook personal computers (PCs).

[0014]Hereinafter, a case where the semiconductor device 1 is mounted on a detachable notebook PC corresponding to the host device 2 will be described with reference to FIGS. 2 and 3. Since the detachable notebook PC is an example of the host device 2, the detachable notebook PC is denoted by the same reference numeral, and described as a detachable notebook PC 2. Further, here, the entire detachable notebook PC 2 connected to the semiconductor device 1 will be described as the system 100. Hereinafter, a description will be made regarding an example where the semiconductor device 1 is mounted on the detachable notebook PC 2.

[0015]FIG. 2 is a diagram when the semiconductor device 1 is mounted on a detachable notebook PC. FIG. 3 is a cross-sectional view of a display unit 110 (a tablet-type portable computer 201) of the detachable notebook PC illustrated in FIG. 2. In the detachable notebook PC, the display unit 110 is connected to a keyboard unit 120 which is a first input receiving device through a connecting portion 130 in a detachable manner from each other. Further, the portable computer 201 and the detachable notebook PC are examples of the host device 2.

[0016]As illustrated in FIGS. 2 and 3, the semiconductor device 1 is mounted on the display unit side of the detachable notebook PC. Therefore, even when being detached, the display unit 110 is allowed to function as the tablet-type portable computer 201, and functions as a second input receiving device.

[0017]The portable computer 201 is an example of electronic equipment, and has, for example, a size such that the user can hold and use by their hand.

[0018]The portable computer 201 includes a housing 202, a display module 203, a semiconductor device 1, and a motherboard 205, as major components. The housing 202 includes a protective plate 206, a base 207, and a frame 208. The protective plate 206 is a square plate made of glass or plastic, and constitutes the surface of the housing 202. The base 207 is made of, for example, metal such as an aluminum alloy or a magnesium alloy, and constitutes the bottom of the housing 202.

[0019]The frame 208 is provided between the protective plate 206 and the base 207. The frame 208 is made of, for example, metal such as an aluminum alloy or a magnesium alloy, and integrally has a mounting portion 210 and a bumper portion 211. The mounting portion 210 is provided between the protective plate 206 and the base 207. According to the present embodiment, a first mounting space 212 is defined between the mounting portion 210 and the protective plate 206, and a second mounting space 213 is defined between the mounting portion 210 and the base 207.

[0020]The bumper portion 211 is formed integrally with the outer peripheral edge of the mounting portion 210, and surrounds continuously the first mounting space 212 and the second mounting space 213 in the circumferential direction. Further, the bumper portion 211 constitutes the outer peripheral surface of the housing 202 while being extended in the thickness direction of the housing 202 in order to extend between the outer peripheral edge of the protective plate 206 and the outer peripheral edge of the base 207.

[0021]The display module 203 is accommodated in the first mounting space 212 of the housing 202. The display module 203 is covered with the protective plate 206, and a touch panel 214 having a handwriting input function is interposed between the protective plate 206 and the display module 203. The touch panel 214 is affixed to the rear surface of the protective plate 206.

[0022]As illustrated in FIG. 3, the semiconductor device 1 and the motherboard 205 are accommodated in the second mounting space 213 of the housing 202. The semiconductor device 1 includes a substrate 11, a NAND memory 12, a controller 13, and other electronic components such as a DRAM 14.

[0023]The substrate 11 is, for example, a printed circuit board, and includes a first surface 11a having a conductor pattern (not illustrated) formed thereon, and a second surface 11b positioned on the opposite side of the first surface 11a. Circuit components are mounted on the first surface 11a and the second surface 11b of the substrate 11, and are soldered to the conductor pattern.

[0024]The motherboard 205 includes substrate 224, and a plurality of circuit component 225 such as a semiconductor package and a chip. The substrate 224 has a plurality of conductor patterns (not illustrated) formed thereon. The circuit component 225 is mounted on the substrate 224, and is electrically connected to the conductor pattern on the substrate 224 through soldering.

[0025]FIGS. 4A to 4C illustrate the appearances of the semiconductor device 1. FIG. 4A is a front view, FIG. 4B is a rear view, and FIG. 4C is a side view. Further, FIG. 5 illustrates a system configuration of the semiconductor device 1.

[0026]As illustrated in FIGS. 4A to 4C, the semiconductor device 1 includes a substrate 11, a NAND type flash memory (hereinafter, abbreviated as a NAND memory) 12 which is a non-volatile semiconductor memory element, a controller 13, a dynamic random access memory (DRAM) 14 which is a volatile semiconductor memory element capable of a faster memory operation than the NAND memory 12, an oscillator 15 (OSC), an electrically erasable and programmable ROM (EEPROM) 16, a power supply circuit 17, a temperature sensor 18, other electronic components 19 such as a resistor and a capacitor, and a pass-through connector 20.

[0027]In addition, the NAND memory 12 and the controller 13 of the present embodiment are mounted as a semiconductor package which is an electronic component. For example, the semiconductor package of the NAND memory 12 is a system-in-package (SiP) type module, and a plurality of semiconductor chips are sealed in one package. The controller 13 controls the operation of the NAND memory 12.

[0028]The substrate 11 is, for example, a substantially rectangular circuit substrate made of material such as glass epoxy resin, and defines the outer dimension of the semiconductor device 1. The substrate 11 includes a first surface 11a, and a second surface 11b positioned on the opposite side of the first surface 11a. In the present specification, surfaces other than the first surface 11a and the second surface 11b, among surfaces constituting the substrate 11, are defined as “side surfaces” of the substrate 11.

[0029]In the semiconductor device 1, the first surface 11a is a component mounting surface on which the NAND memory 12, the controller 13, the DRAM 14, the oscillator 15, the EEPROM 16, the power supply circuit 17, the temperature sensor 18, and other electronic components 19 such as a resistor and a capacitor are mounted.

[0030]Meanwhile, in the present embodiment, the second surface 11b of the substrate 11 is a non-component mounting surface on which components are not mounted. Thus, most of a plurality of components which are provided independently of the substrate 11 are disposed on one surface of the substrate 11, thereby allowing most components to protrude from the surface of the substrate 11 only on one surface side of the substrate 11. This enables reduction in the thickness of the semiconductor device 1, as compared to the case where components protrude from both the first surface 11a and the second surface 11b of the substrate 11.

[0031]As illustrated in FIGS. 4A to 4C, the substrate 11 includes a first edge portion 11c, and a second edge portion 11d positioned on the opposite side of the first edge portion 11c. The first edge portion 11c includes an interface unit 21 (a substrate interface unit, a terminal portion, and a connecting portion).

[0032]The interface unit 21 includes, for example, a plurality of connection terminals 21a (metal terminals). The interface unit 21 is inserted into, for example, the connector 3 of the host device 2, and is electrically connected to the connector 3. The interface unit 21 exchanges signals (a control signal and a data signal) between the interface unit 21 and the host device 2. Further, here, the host device 2 is, for example, the portable computer 201 described above.

[0033]The interface unit 21 according to the present embodiment is, for example, an interface conforming to, for example, the PCI Express (hereinafter, PCIe) standard. In other words, high-speed signals (high-speed differential signals) conforming to the PCIe standard flow between the interface unit 21 and the host device 2. Further, the interface unit 21 may conform to, for example, other standards such as serial advanced technology attachment (SATA), universal serial bus (USB), and serial attached SCSI (SAS). The semiconductor device 1 is supplied with power from the host device 2 through the interface unit 21.

[0034]A slit 21b is formed at a position shifted from the center position in the widthwise direction of the substrate 11, in the interface unit 21, and fits the projections (not illustrated) and the like formed on the connector 3 side of the host device 2. This makes it possible to prevent the semiconductor device 1 from being mounted in a front and rear reversed manner.

[0035]The power supply circuit 17 is, for example, a DC-DC converter, and generates a predetermined voltage, which is required for the semiconductor package 10 and the like, from the power supplied from the host device 2. Further, it is desirable that the power supply circuit 17 is installed in the vicinity of the interface unit 21 in order to suppress the loss of the power supplied from the host device 2.

[0036]The controller 13 controls the operation of the NAND memory 12. In other words, the controller 13 controls the writing data to, and the reading and erasing data from the NAND memory 12.

[0037]The DRAM 14 is an example of a volatile memory, and is used for storage of management information of the NAND memory 12, data cache, and the like. For example, other volatile memories such as an SRAM may be used for the DRAM 14.

[0038]The oscillator 15 supplies an operation signal of a predetermined frequency to the controller 13. The EEPROM 16 stores a control program or the like as fixed data.

[0039]The temperature sensor 18 notifies the controller 13 of the temperature of the semiconductor device 1. Further, in the present embodiment, a single temperature sensor 18 is mounted on the substrate 11, and the temperature of the semiconductor device 1 is monitored by the temperature sensor 18.

[0040]In the present embodiment, a plurality of types of electronic components such as the NAND memory 12, the controller 13, and the DRAM 14 are mounted on the substrate 11, and the respective temperatures differ depending on the operation state of the semiconductor device 1, the loads applied to the respective electronic components, and the like. Therefore, strictly, the temperature of the semiconductor device 1 is not uniform.

[0041]Thus, in the present embodiment, “the temperature of the semiconductor device 1” is defined as a temperature measured in the position where the temperature sensor 18 is mounted. In other words, in the present embodiment, “the temperature of the semiconductor device 1” is a temperature around the mounting position of the temperature sensor 18.

[0042]Further, the number of temperature sensors 18 needs not necessarily one, and for example, it may be configured such that a plurality of temperature sensors 18 are provided in the substrate 11, and the temperatures of a plurality of positions are monitored. Further, the temperature sensor 18 needs not necessarily be provided on the substrate 11, and may be provided as the function of the controller 13.

[0043]Further, the temperature sensor 18 may be mounted in the package interior such as the NAND memory 12 and the controller 13, and may be provided so as to be affixed to the package surface. In this case, the temperature sensor 18 can measure more accurately the temperature of a single NAND memory 12 and the temperature of a single controller 13.

[0044]The pass-through connector 20 is provided, for example, in the first surface 11a of the substrate 11 to allow the connection between the semiconductor device 1 and other semiconductor devices. The semiconductor device 1 is connectable to other semiconductor devices through the harness 4 (later illustrated in FIG. 8) connected to the pass-through connector 20.

[0045]In the present embodiment, the number, the mounting positions, and the like of NAND memories 12 are not limited to the drawings. For example, the present embodiment illustrates an example in which two NAND memories 12 (12a and 12b) are mounted on the first surface 11a of the substrate 11, but for example, the number of NAND memories 12 is not limited.

[0046]FIG. 6 illustrates a cross-section, in which a semiconductor package as the NAND memory 12 and a semiconductor package as the controller 13 in the present embodiment are illustrated. The controller 13 includes a package substrate 41, a controller chip 42, a bonding wire 43, a sealing portion (mold material) 44, and a plurality of solder balls 45. The NAND memory 12 includes a package substrate 31, a plurality of memory chips 32, a bonding wire 33, a sealing portion (mold material) 34, and a plurality of solder balls 35.

[0047]The substrate 11 is, for example, a multi-layer wiring substrate, as described above, includes a power layer, a ground layer, and an internal wiring, which are not illustrated, and is connected to the controller chip 42 and the plurality of semiconductor memories 32, through the bonding wires 33 and 43, the plurality of solder balls 35 and 45, and the like.

[0048]As illustrated in FIG. 6, the plurality of solder balls 35 and 45 are provided on the package substrates 31 and 41. The plurality of solder balls 35 and 45 are arranged, for example, in a lattice pattern on the second surface 31b of the package substrate 31. In addition, the plurality of solder balls 35 need not to be placed in full on the entire second surface 31b of the package substrate 31, and may be partially placed.

[0049]Further, the package substrates 31 and 41 are respectively fixed to the controller chip 42 and the semiconductor memory 32, and the plurality of semiconductor memories 32 are fixed with each other through mounting films 38 and 48.

[0050]In addition, after the mounting films 38 and 48 are respectively affixed to the package substrates 31 and 41, the memory chip 32 and the controller chip 42 may be mounted. Further, for example, an individual chip piece (controller chip 42) may be made by affixing the mounting film 48 to a wafer used for the controller chip 42, and dicing the wafer. The same is applied to the memory chip 32 and the mounting film 38.

[0051]As illustrated in FIGS. 4A to 4C, the controller 13 of the present embodiment has a substantially rectangular shape, and includes a first edge portion in a widthwise direction, a second edge portion positioned on the opposite side of the first edge portion, a third edge portion in a longitudinal direction, and a fourth edge portion positioned on the opposite side of the third edge portion. Further, the second edge portion is positioned on the NAND memory 12 side that is mounted on the substrate 11 adjacent to the controller 13, and the first edge portion is positioned on the interface unit 21 side included in the substrate 11.

[0052]Further, the afore-mentioned solder ball 45 includes a solder ball 45a present on the first edge portion side of the controller 13 and a solder ball 45b present on the second edge portion side. Further, the solder ball 35 includes a solder ball 35a positioned on the controller 13 side, and a solder ball 35b positioned on the opposite side of the solder ball 35a.

[0053]FIG. 7 is an example of a system configuration of the controller 13. As illustrated in FIG. 7, the controller 13 includes a buffer 131, a central processing unit (CPU) 132, a host interface unit 133, and a memory interface unit 134.

[0054]Further, as described above, the controller 13 may be provided with, for example, the function of the temperature sensor 18, and the function of the power supply circuit 17, and the system configuration of the controller 13 is not limited thereto.

[0055]When writing data sent from the host device 2 to the NAND memory 12, the buffer 131 temporarily stores a certain amount of data; and when sending data read from the NAND memory 12 to the host device 2, the buffer 131 temporarily stores a certain amount of data.

[0056]The CPU 132 controls the entire semiconductor device 1. The CPU 132 includes a CPU 132, a control unit 135, and a switching unit 136.

[0057]The control unit 135 receives, for example, a write command, a read command, and an erase command from the host device 2, accesses the corresponding region of the NAND memory 12, or controls a data transfer process through the buffer 131.

[0058]The switching unit 136 switches the operation mode of the controller 13. Specifically, switching unit 136 receives a command from the host device 2, and performs an operation switching between a normal mode and a pass-through mode. Further, the normal mode and the pass-through mode will be described later.

[0059]The host interface unit 133 is positioned between the interface unit 21 of the substrate 11, and the CPU 132 and the buffer 131. The host interface unit 133 performs an interface process between the controller 13 and the host device 2. For example, PCIe high-speed signals flow between the host interface unit 133 and the host device 2.

[0060]Further, the host interface unit 133 is disposed in the direction of the interface unit 21 of the substrate 11, in other words, so as to be closer to the first edge portion, in the controller 13. In this case, it is possible to shorten the wiring between the host interface unit 133 and the interface unit 21 of the substrate 11.

[0061]For example, if the host interface unit 133 is disposed in the opposite direction of the interface unit 21, in other words, so as to be closer to the second edge portion, in the controller 13, as can be seen from FIGS. 4A to 4C, the wiring distance connecting the interface unit 21 and the host interface unit 133 is extended by the length in the longitudinal direction of the controller chip. Since the wiring becomes long and parasitic capacitance, parasitic resistance, parasitic inductance, and the like increase, it is difficult to maintain the characteristic impedance of a signal wiring. This can be a cause of signal delay.

[0062]From the above viewpoint, in the present embodiment, it is desirable that the host interface unit 133 is disposed closer to the first edge portion in the controller 13, and for example, when a command is sent from the host device 2, the interface unit 21 receives signals from the host device 2, and exchanges signals with the host interface unit 133 from the wiring pattern of the substrate 11 through the solder ball 45a. Thus, the improvement of the operation stability of the semiconductor device 1 is achieved.

[0063]Further, it is desirable that electronic components are not mounted between the host interface unit 133, and the interface unit 21 of the substrate 11.

[0064]As described above, when the wiring distance between the host interface unit 133 and the interface unit 21 is long, there is a problem in that it is difficult to maintain the impedance of a signal wiring, and causes a signal delay. Thus, it is desirable that electronic components are mounted between the host interface unit 133 and the interface unit 21 in order to perform a wiring connecting the host interface unit 133 and the interface unit 21 at the shortest distance, in other words, linearly.

[0065]There is a possibility that the power supply circuit 17 and the electronic component such as the DRAM 14 involve noise during the operation. Since these electronic components are not mounted between the host interface unit 133 and the interface unit 21, the signals exchanged between the host interface unit 133 and the interface unit 21 are less likely to pick up noise, and the improvement of the operation stability of the semiconductor device 1 can be achieved.

[0066]The memory interface unit 134 is positioned between the NAND memory 12, and the CPU 132 and the buffer 131. The memory interface unit 134 performs an interface process between the controller 13 and the NAND memory 12.

[0067]In the present embodiment, the memory interface unit 134 is disposed in the direction of the opposite side of the interface unit 21 of the substrate 11, in other words, so as to be closer to the second edge portion, in the controller 13. In this case, it is possible to shorten the wiring distance between the memory interface unit 134 and the NAND memory 12.

[0068]The signal sent from the controller 13 is transmitted to the wiring pattern of the substrate 11 through the solder ball 45b, and is transmitted from the solder ball 35a to the memory chip 32. Thus, the wiring distance is reduced, and the improvement of the operation stability of the semiconductor device 1 is achieved.

[0069]Further, it is desirable that electronic components such as the power supply circuit 17 and the DRAM 14 are not also mounted between the memory interface unit 134 of the controller 13 and the NAND memory 12 on the substrate 11. This is because signals exchanged between the memory interface unit 134 and the interface unit 21 are less likely to pick up noise, and the improvement of the operation stability of the semiconductor device 1 is achieved.

[0070]FIG. 8 is a diagram illustrating a connection relationship between the semiconductor devices 1 according to the present embodiment. Further, here, an example is illustrated in which a semiconductor device 1a and a semiconductor device 1b are connected. For convenience of explanation, in FIG. 8, the configuration of a portion of the semiconductor device 1a and the semiconductor device 1b is not illustrated.

[0071]Further, a pass-through connector 20a, a controller 13a, and a NAND memory 12a are provided in the semiconductor device 1a; and a pass-through connector 20b, a controller 13b, and a NAND memory 12b are provided in the semiconductor device 1b.

[0072]Further, in the following description, for example, the contents of those expressed as “pass-through connector 20” can be applied to a pass-through connector 20a and a pass-through connector 20b. The same is applied to the semiconductor device 1, the controller 13, and the NAND memory 12.

[0073]As illustrated in FIG. 8, in the present embodiment, the semiconductor device 1a and the semiconductor device 1b are connected through the pass-through connector 20 and harnesses 4. The number of harnesses 4 and the position of the pass-through connector 20 are not limited to FIG. 8.

[0074]The pass-through connector 20 is connected to the internal wiring (not illustrated) of the substrate 11 connecting the controller 13 and the NAND memory 12. Further, a connecting method between the controller 13 and the NAND memory 12 is not limited to the internal wiring of the substrate 11.

[0075]Here, it is assumed that controller 13b is no longer functioning due to the failure of the semiconductor device 1b. In the present embodiment, the semiconductor device 1b includes the pass-through connector 20b, and is connected to the semiconductor device 1a through the harness 4. Since the controller 13b does not function in the semiconductor device 1b, it is not possible to read the data stored in the NAND memory 12b by using the controller 13b.

[0076]Thus, the controller 13 in the present embodiment is capable of performing two types of operations of the normal mode and the pass-through mode.

[0077]In the normal mode, for example, the command and data supplied from the host device 2 is subjected to an input and output process and a required local-physical address conversion process by the controller 13a, and then stored (written) in the NAND memory 12a. Further, the data read from the NAND memory 12a is also subjected to the input and output process by the controller 13a, and read on the host device 2 side. The same is applied to the semiconductor device 1b. Incidentally, the controller 13a is typically operated in the normal mode.

[0078]Meanwhile, in the pass-through mode, the controller 13a is accessible to the NAND memory 12b of the semiconductor device 1b through the pass-through connector 20 and the harness 4. Incidentally, the controller 13 is typically operated in the normal mode, but is switched to the pass-through mode under predetermined conditions (according to predetermined input, command, and the like). Here, the predetermined input, command, and the like are given, for example, from the host device 2.

[0079]In the pass-through mode, the controller 13a accesses the NAND memory 12b of the semiconductor device 1b, and is capable of reading the data stored in the NAND memory 12b. Thus, it is possible to save data from the failed semiconductor device 1b.

[0080]FIG. 9 is a flowchart illustrating an example of the operation of the controller 13a during data saving of the semiconductor device 1b according to the present embodiment. Further, it is assumed that the semiconductor device 1 is failed, and a description will be made from the state where the host device 2 recognizes the failure of the semiconductor device 1b.

[0081]The controller 13a receives a command from the host device 2 (Step 1.1). Here, the command requests the controller 13a to perform switching to the pass-through mode.

[0082]The controller 13a that receives the command checks if switching from the normal mode to the pass-through mode is possible (Step 1.2). While the semiconductor device 1 processes data in the normal mode (for example, when writing data to the NAND memory 12a, or when reading data from the NAND memory 12a), the controller 13a is on standby until switching to the pass-through mode is possible.

[0083]When the switching to the pass-through mode is possible, the controller 13a proceeds to the pass-through mode, and accesses the NAND memory 12b of the semiconductor device 1b. Thereafter, data is read from the NAND memory 12b, and data is stored in the buffer 131a of the controller 13 (Step 1.3).

[0084]Next, the controller 13a checks if writing to the NAND memory 12a is possible (Step 1.4). In other words, the controller 13a checks if there is a free space for writing the data that is saved from the NAND memory 12b to the NAND memory 12a.

[0085]When there is a free space in the NAND memory 12a, the controller 13a reads data stored in the buffer 131a in Step 1.3, writes the data to the NAND memory 12a, and ends the saving of the data (Step 1.5).

[0086]In contrast, when the writing to the NAND memory 12a is not possible, the controller 13a reads data stored in the buffer 131a in Step 1.3, transmits the data to the host device 2, and ends the saving of the data (Step 1.6). The host device 2 that receives data in Step 1.6 may store data, for example, in other storage devices such as an SSD, a hard disk drive (HDD), a USB memory, or an SD card.

[0087]Further, when there is no free space (free block) in the NAND memory 12a in Step 1.4, a free space may be created in the NAND memory 12a, for example, by a process such as garbage collection.

[0088]The garbage collection is an operation for creating a free space. Since the garbage collection operation increases the number of free blocks in the NAND memory 12a, valid data is aggregated by using a plurality of erase blocks in which valid data and invalid data are mixed.

[0089]In the garbage collection operation, valid data is read from a group of erase blocks in which valid data and invalid data are mixed, and the valid data is written to a certain erased block. As a result, the valid data is collected in a specific some erase blocks, and a group of erase blocks including only invalid data is reusable as free blocks.

[0090]Through the above operation, a region for data saving of the NAND memory 12b is secured in the NAND memory 12a, in which data saving may be performed therein.

[0091]Here, in the present embodiment, the case is considered where the pass-through connector 20 is not provided in the semiconductor device 1. In this case, when the semiconductor device 1 is failed, it is not possible to access the NAND memory 12b, and it is not possible to read data stored in the NAND memory 12b.

[0092]Further, if a pass-through terminal (a terminal for accessing directly the NAND memory 12 without passing through the controller 13) is provided in the semiconductor device 1, it is possible to read data by using, for example, an external reading device, but generally a device dedicated for reading used in such application is often expensive.

[0093]Thus, in the present embodiment, the semiconductor device 1a includes a pass-through connector 20, and the controller 13a is switched to the pass-through mode, such that it is possible to directly access the NAND memory 12b mounted in the semiconductor device 1b.

[0094]Therefore, it is possible to directly access the NAND memory 12b in which data to be retracted is stored, and it is possible to directly save the data to the NAND memory 12a of the semiconductor device 1a. Therefore, since it is not necessary to pass through the host device 2 and other external devices, it is possible to simplify the process of data saving. In addition, since data is exchanged in the semiconductor devices 1 with each other, there is no need to use an expensive device such as an external reading device.

[0095]Incidentally, in the present embodiment, the pass-through connector 20 is only an example of a unit that connects the semiconductor device 1a and the semiconductor device 1b, and for example, as in FIG. 10, it may be configured such that various control signals and various input and output port signals are connected by a plurality of connecting units.

Second embodiment

[0096]FIGS. 11A to 11C illustrate appearances of a semiconductor device 1 according to the present embodiment, FIG. 11A is a front view, FIG. 11B is a rear view, and FIG. 11C is a side view. Further, FIG. 12 is a diagram illustrating a configuration during connection between a semiconductor devices 1a and a semiconductor device 1b according to the second embodiment. Further, in the description of the present embodiment, the same components as in the first embodiment are denoted by the same reference numerals, and the detailed description thereof will be omitted.

[0097]As illustrated in FIGS. 11A to 11C, the semiconductor device 1 according to the present embodiment includes a power supply terminal 60 and a pass-through terminal 50 on the second surface 11b of the substrate 11. The power supply terminal 60 is a terminal for starting the semiconductor device 1, and is capable of supplying power, for example, from the outside. The pass-through terminal 50 enables the direct access to the NAND memory 12 from the outside.

[0098]The pass-through terminal 50 is connected to at least a portion of the internal wiring (not illustrated) of the substrate 11 that is connected to the controller 13 and the NAND memory 12. Further, a method of connecting the controller 13 and the NAND memory 12 is not limited to the internal wiring of the substrate 11.

[0099]As illustrated in FIG. 12, the semiconductor device 1 in the present embodiment is connected to the pass-through device 300. The pass-through device 300 includes a pass-through connector 20, a start connector 25, a base board 30, a start pin 70, and a pass-through pin 40.

[0100]The base board 30 is, for example, a substantially rectangular circuit substrate made of a material such as glass epoxy resin. The base board 30 is, for example, a multi-layer wiring substrate, and includes a ground layer, a power layer, and a wiring layer.

[0101]The start connector 25 is connected to, for example, the host device 2, and supplies power from the host device 2 to the semiconductor device 1. The start connector 25 is provided on the base board 30, and is electrically connected to the start pin 70 by an internal wiring (not illustrated).

[0102]The start pin 70 is a contact probe pin provided on the base board 30, and is connected to the power supply terminal 60 provided on the second surface 11b of the semiconductor device 1.

[0103]The pass-through pin 40 is a contact probe pin provided on the base board 30, and is connected to the pass-through terminal 50 provided on the second surface 11b of the semiconductor device 1.

[0104]Further, the start pin 70 and the pass-through pin 40 need not necessarily be the projecting contact probe pin, and for example may be connected to the semiconductor device 1 as a socket-like configuration.

[0105]The pass-through connector 20 is provided on the base board 30, and is electrically connected to the pass-through pin 40 by an internal wiring (not illustrated).

[0106]In addition, the configurations described above are common to the semiconductor device 1a and the semiconductor device 1b, and the pass-through device 300a and the pass-through device 300b.

[0107]The semiconductor device 1a and the semiconductor device 1b are connected through the harness 4. Specifically, the harness 4 is connected to the pass-through connector 20a provided in the pass-through device 300a to which the semiconductor device 1a is connected, and the pass-through connector 20b provided in the pass-through device 300b to which the semiconductor device 1b is connected.

[0108]With the above configuration, for example, when the semiconductor device 1b is failed, the semiconductor device 1a of the present embodiment directly accesses the NAND memory 12b of the semiconductor device 1b, and is capable of reading data of the NAND memory 12b, similar to the first embodiment.

[0109]Further, in the present embodiment, the pass-through connector 20 is not provided on the semiconductor device 1, but rather the pass-through device 300 is provided therein. Thus, it is not necessary to secure a mounting space for the pass-through connector 20 in the semiconductor device 1, and it is possible to suppress the size expansion of the semiconductor device 1.

[0110]In addition, in the present embodiment, the pass-through terminal 50 is provided on the second surface 11b of the substrate 11 of the semiconductor device 1. Therefore, it is not necessary to consider a space or the like for mounting the pass-through terminal 50, the pass-through connector 20, and the like, when mounting respective components on the first surface 11a which is a component mounting surface.

[0111]Further, in the present embodiment, at least as long as the pass-through terminal 50a and the pass-through terminal 50b which are provided in the semiconductor device 1a and semiconductor device 1b are connected to each other and power is supplied to the semiconductor device 1a and the semiconductor device 1b, it needs not necessarily use the pass-through device 300 as illustrated in FIG. 12.

[0112]The above describes the first embodiment and the second embodiment, but the terms and the like used in the description are not limited thereto. For example, since the pass-through connector 20, the pass-through terminal 50, and the like as described above connect the semiconductor device 1a and the semiconductor device 1b, they may collectively be referred to as a connecting portion.

[0113]From the above, “connecting portion” may be configured such that the controller 13a of the semiconductor device 1a is able to directly access the NAND memory 12b (data stored in the NAND memory 12b) of the semiconductor device 1b. Further, “directly” described above refers to access without passing through, for example, the host device 2, the controller 13b, and the like.

[0114]Therefore, for example, in the first embodiment, the semiconductor device 1a and the semiconductor device 1b may be connected, for example, in a wireless manner. In other words, “connecting” includes not only wiring, but also wireless connection. Further, in this case, the connecting portion needs not necessarily be provided on the substrate 11, and for example, the connecting portion may be provided as a part of the functions of the controller 13, or may be provided in the package of the NAND memory 12.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first substrate on which an interface unit connectable to a host device is provided;

a first memory that is mounted on the first substrate;

a first controller that is mounted on the first substrate, and includes a control unit which controls the first memory, and a switching unit which switches an operation mode in response to a command from the host device; and

a first connecting portion that is provided on the first substrate, and is electrically connected to the first memory and the first controller,

wherein the first controller accesses an external second memory through the first connecting portion, and reads data stored in the second memory, in response to the switching by the switching unit.

2. The device according to Claim 1,

wherein the first controller writes the data that is read from the second memory, to the first memory.

3. The device according to Claim 2,

wherein the first controller checks if writing to the first memory is possible, in response to reading of the data from the second memory, and when the writing is possible, the first controller writes the data that is read from the second memory, to the first memory.

4. The device according to Claim 2 or 3,

wherein the first controller checks if writing to the first memory is possible, in response to reading of the data from the second memory, and when the writing is not possible, the first controller transmits the data that is read from the second memory, to the host device.

5. The device according to Claim 2 or 3,

wherein the first controller checks if writing to the first memory is possible, in response to reading of the data from the second memory, and when the writing is not possible, the first controller performs a garbage collection process of the first memory, and writes the data that is read from the second memory to the first memory.

6. The device according to any one of Claims 1 to 5,

wherein the second memory is mounted on a second substrate having a second controller mounted thereon,

wherein the second substrate includes a second connecting portion that is electrically connected to the second memory and the second controller, the first connecting portion and the second connecting portion being electrically connected with each other.

7. A semiconductor device comprising:

a first memory;

a controller that controls the first memory;

a wiring that electrically connects the first memory and the controller; and

a connecting portion that is connected to the wiring,

wherein the controller is accessible to a second memory through the connecting portion.

8. A semiconductor device comprising:

a first memory;

a controller that accesses the first memory, and performs switching to access to a second memory under a predetermined condition; and

a connecting portion that is connectable to the second memory.

ABSTRACT

According to one embodiment, provided is a semiconductor device including a first substrate on which an interface unit connectable to a host device is provided; a first memory that is mounted on the first substrate; a first controller that is mounted on the first substrate and includes a control unit which controls the first memory, and a switching unit which switches an operation mode in response to a command from the host device; and a first connecting portion that is provided on the first substrate, and is electrically connected to the first memory and the first controller, in which the first controller accesses an external second memory through the first connecting portion, and reads data stored in the second memory, in response to the switching by the switching unit.

FIG. 5

2 HOST DEVICE

17 POWER SUPPLY CIRCUIT

13 CONTROLLER

18 TEMPERATURE SENSOR

12 NAND MEMORY

FIG. 7

134 MEMORY INTERFACE UNIT

135 CONTROL UNIT

136 SWITCHING UNIT

131 BUFFER

133 HOST INTERFACE UNIT

Fig. 8

2 host device

1a, 1b semiconductor device

13a ,13b controller

12a, 12b nand memory

Fig. 9

Step1.1 receive command from host device

Step1.2 is switching to paSS-through mode possible?

Step1.3 read data from NAND memory 12b, write data to buffer

Step1.4 is writing to NAND memory 12a possible?

Step1.5 save data to NAND memory 12a

Step1.6 transmit data to host device 2

Fig. 10

2 host device

1a, 1b semiconductor device

13a ,13b controller

input and output signals

control signals

12a, 12b nand memory